We claim:

1. A MOS transistor, comprising:

a gate structure formed over a semiconductor;

source and drain regions formed in said semiconductor;

drain and source extension regions formed in said semiconductor adjacent said gate structure and positioned between said gate structure and said source and drain regions; and

first metal silicide layers formed on said drain and source extension regions.

2. The MOS transistor of claim 1 further comprising sidewall structures adjacent said gate structure and over said first metal silicide layers.

3. The MOS transistor of claim 2 further comprising second metal silicide layers formed on said source and drain regions.

4. The MOS transistor of claim 1 wherein said first metal silicide layer is selected from the group consisting of cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.

5. The MOS transistor of claim 2 wherein said drain and source extension regions have a first doping concentration and said drain and source regions have a second doping concentration such that said second doping concentration is greater than said first doping concentration.

6. The MOS transistor of claim 5 wherein said drain and source extension regions extend to a first depth and said drain and source regions extend to a second depth such that said second depth is greater than said first depth.

7. An integrated circuit MOS transistor, comprising:

a gate structure formed over a semiconductor;

sidewall structures formed adjacent said gate structure;

a semiconductor layer formed above said semiconductor adjacent to said sidewall structure;

source and drain regions formed adjacent to said sidewall structures in said semiconductor layer and said semiconductor;

drain and source extension regions formed in said semiconductor adjacent said gate structure and positioned substantially beneath said sidewall structures; and

first metal silicide layers formed on said drain and source extension regions.

8. The MOS transistor of claim 7 further comprising second metal silicide layers formed on said source and drain regions.

9. The MOS transistor of claim 7 wherein said first metal silicide layer is selected from the group consisting of cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.

10. The MOS transistor of claim 7 wherein said drain and source extension regions have a first doping concentration and said drain and source regions have a second doping concentration such that said second doping concentration is greater than said first doping concentration.

11. The MOS transistor of claim 10 wherein said drain and source extension regions extend to a first depth and said drain and source regions extend to a second depth such that said second depth is greater than said first depth.

12. A method for forming a MOS transistor, comprising:

forming a gate structure over a semiconductor;

forming source and drain regions in said semiconductor;

forming drain and source extension regions in said semiconductor adjacent said gate structure and positioned between said gate structure and said source and drain regions; and

forming first metal silicide layers on said drain and source extension regions.

13. The method of claim 12 further comprising forming sidewall structures adjacent said gate structure and over said first metal silicide layers.

14. The method of claim 13 further comprising forming second metal silicide layers on said source and drain regions.

15. The method of claim 12 wherein said first metal silicide layer is formed from the group consisting of cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.

16. The method of claim 12 wherein said drain and source extension regions are formed using with a first doping concentration and said drain and source regions are formed using a second doping concentration such that said second doping concentration is greater than said first doping concentration.

17. The method of claim 16 wherein said drain and source extension regions are formed to extend to a first depth and said drain and source regions extend to a second depth such that said second depth is greater than said first depth.

18. An integrated circuit MOS transistor, comprising:

forming a gate structure over a semiconductor;

forming sidewall structures adjacent said gate structure;

forming a semiconductor layer above said semiconductor adjacent to said sidewall structure;

forming source and drain regions adjacent to said sidewall structures in said semiconductor layer and said semiconductor;

forming drain and source extension regions in said semiconductor adjacent said gate structure and positioned substantially beneath said sidewall structures; and

forming first metal silicide layers on said drain and source extension regions.

19. The method of claim 18 further comprising forming second metal silicide layers on said source and drain regions.

20. The method of claim 18 wherein said first metal silicide layer is formed from the group consisting of cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.

21. The method of claim 18 wherein said drain and source extension regions are formed with a first doping concentration and said drain and source regions are formed with a second doping concentration such that said second doping concentration is greater than said first doping concentration.

22. The method of claim 21 wherein said drain and source extension regions are formed to a first depth and said drain and source regions are formed to a second depth such that said second depth is greater than said first depth.